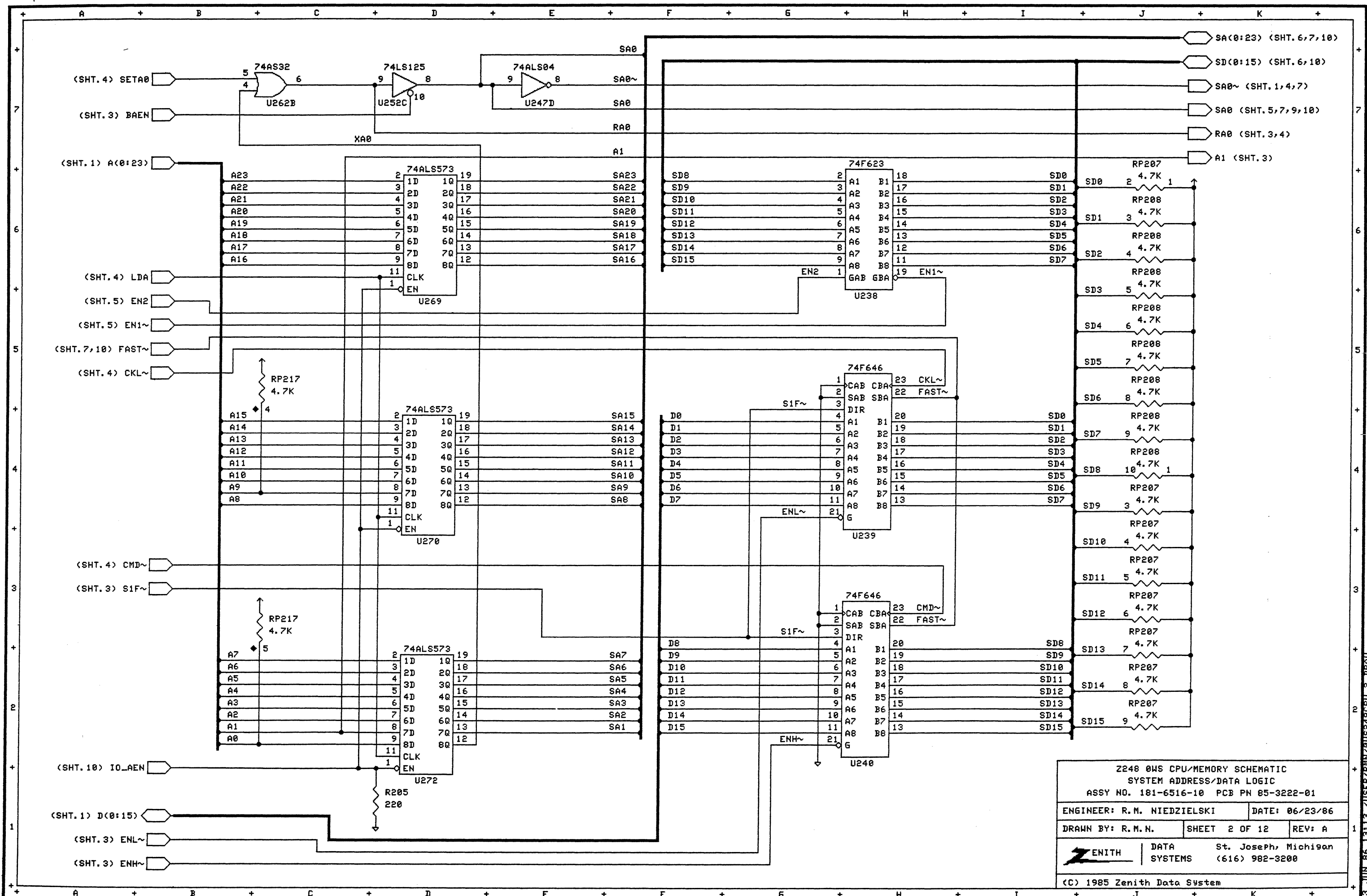


Z248 0WS CPU/MEMORY SCHEMATIC  
CPU/COPROCESSOR LOGIC  
ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R.M. NIEDZIELSKI	DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 1 OF 12 REV: A
<b>ZENITH</b> DATA SYSTEMS    St. Joseph, Michigan (616) 982-3200	
(C) 1985 Zenith Data System	

19 AUG 86 09:33 USER:RMN/QWS248CPU I.DRAW



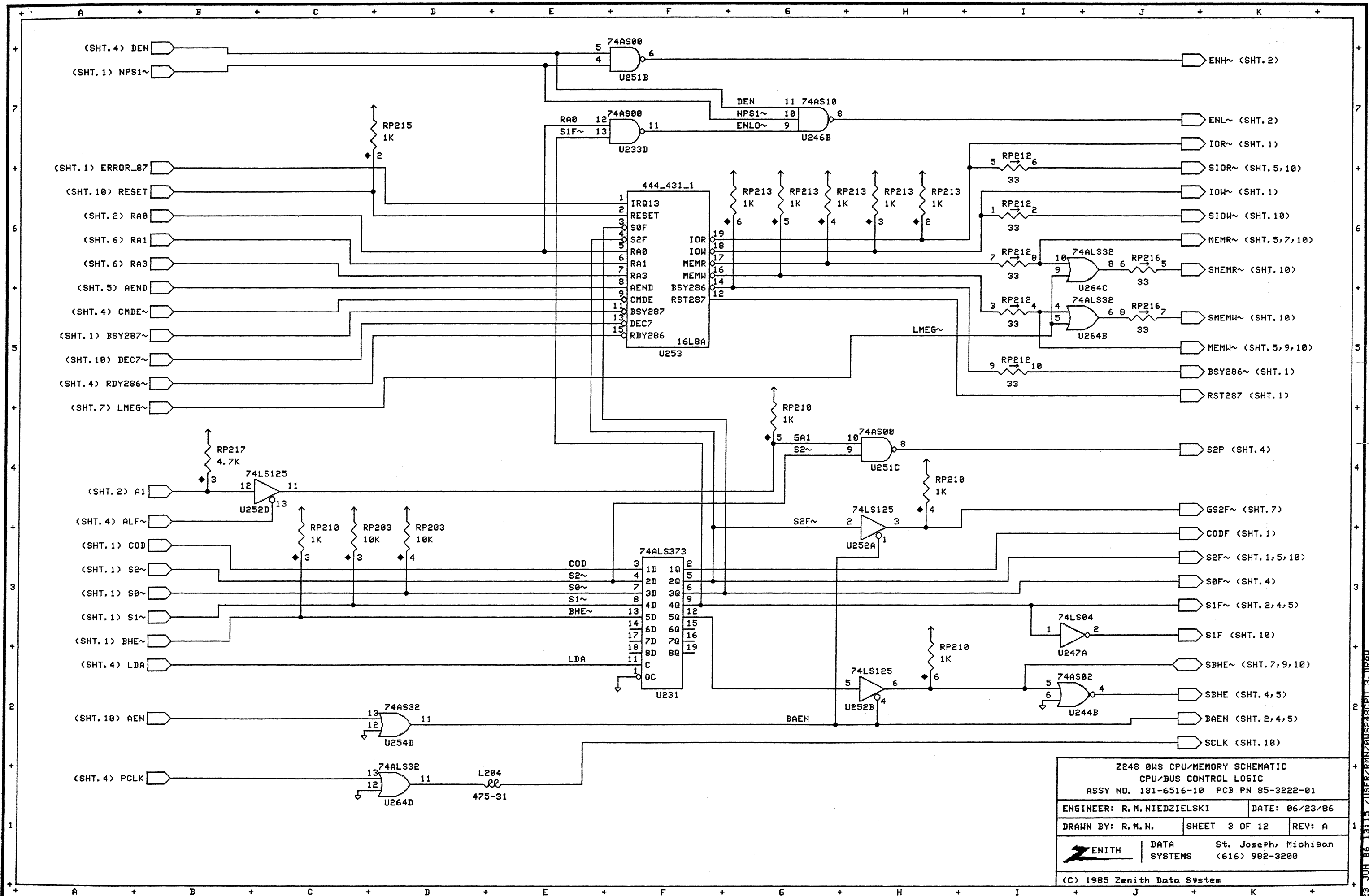
Z248 CPU/MEMORY SCHEMATIC  
SYSTEM ADDRESS/DATA LOGIC  
ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 2 OF 12 REV: A

**ZENITH** DATA St. Joseph, Michigan  
SYSTEMS (616) 982-3200

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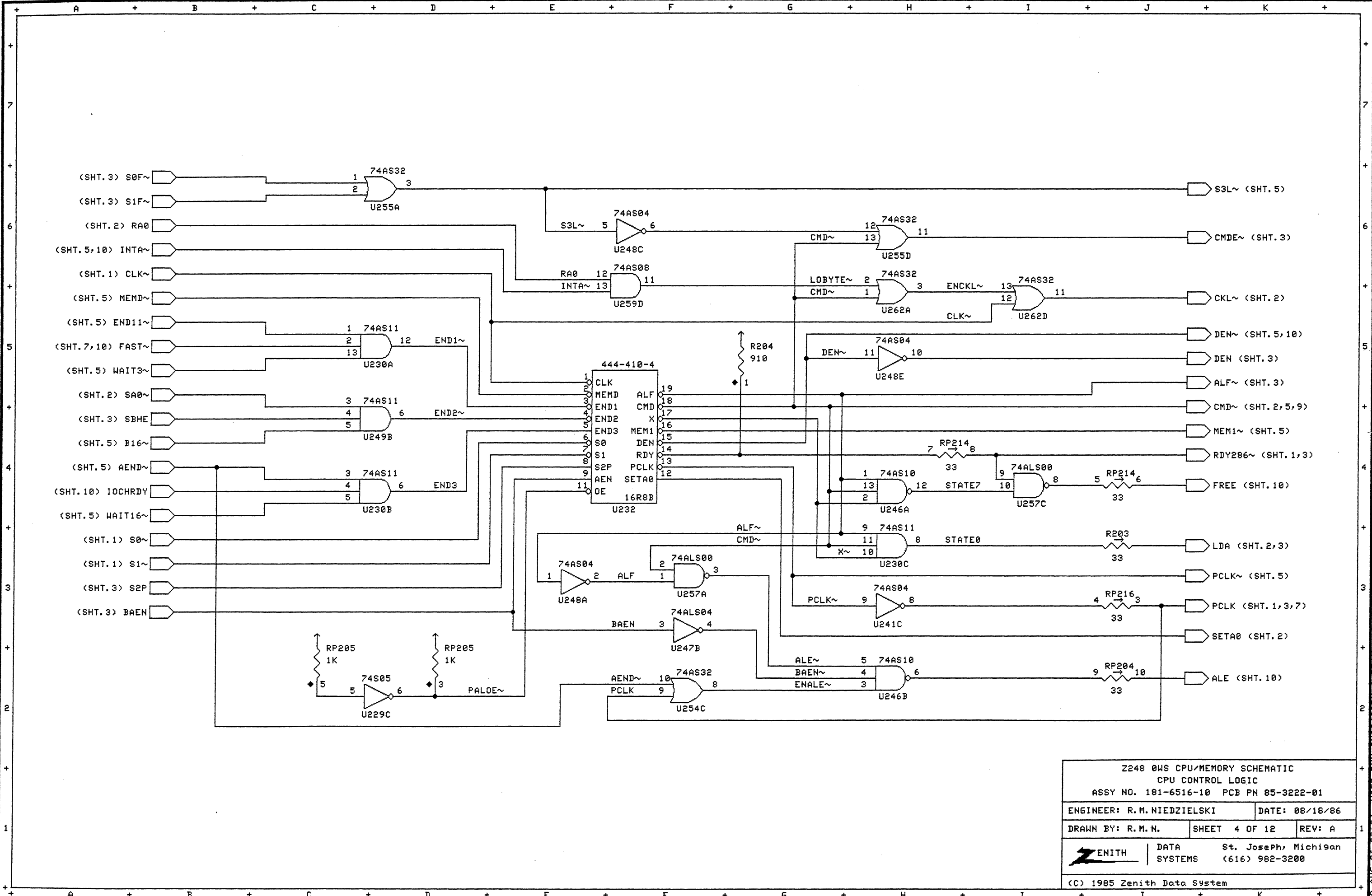
23 JUN 86 13:13 USER:RMN/048248CPU 2. DRAM



Z248 0WS CPU/MEMORY SCHEMATIC  
 CPU/BUS CONTROL LOGIC  
 ASSY NO. 181-6516-10 PCB PN 85-3222-01

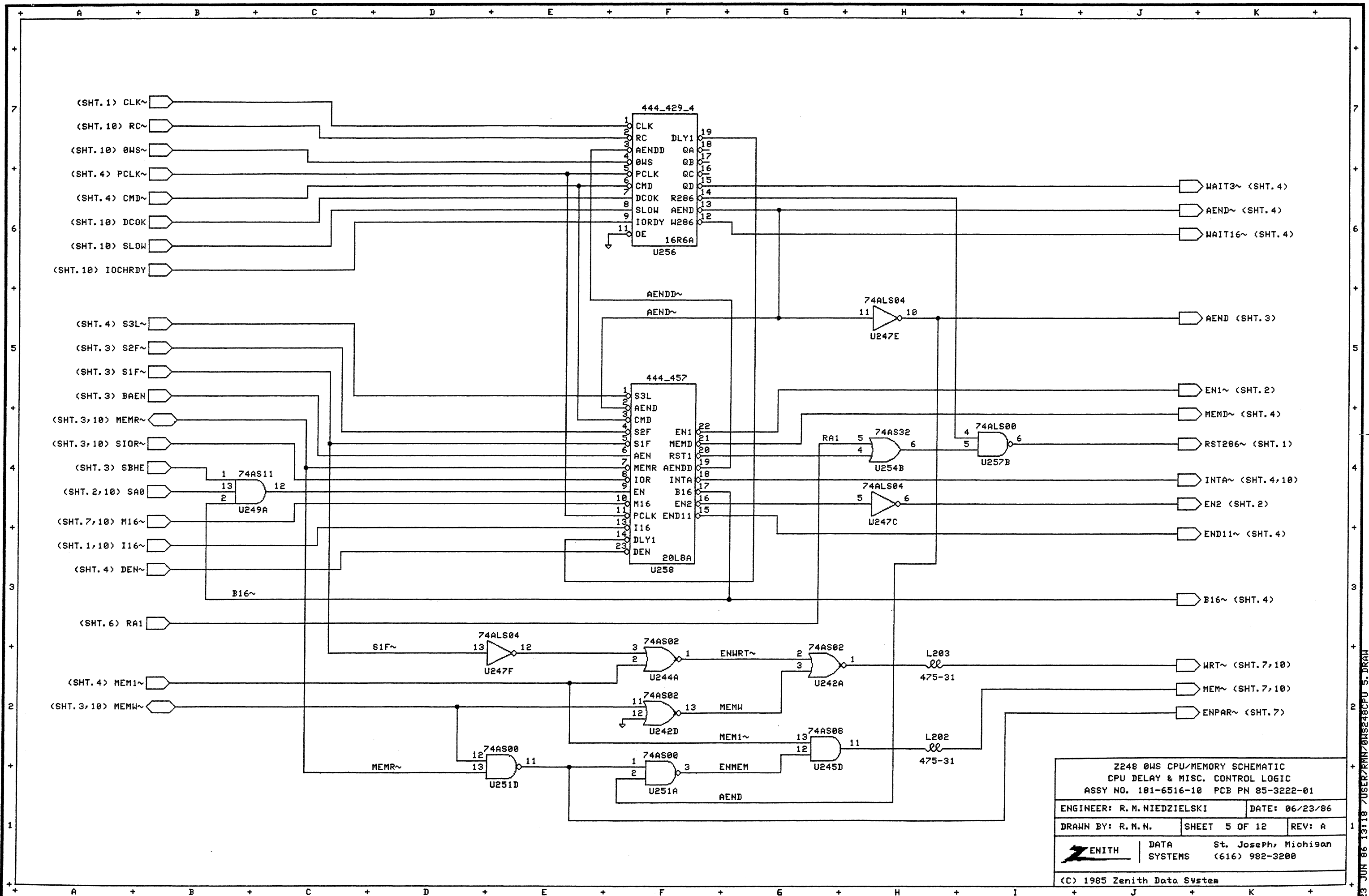
ENGINEER: R.M.NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R.M.N.	SHEET 3 OF 12
DATA St. Joseph, Michigan SYSTEMS (616) 982-3200	
(C) 1985 Zenith Data System	

23 JUN 86 13:15 USER:RMN/0WS248CPU 3.DRAW



2248 OWS CPU/MEMORY SCHEMATIC CPU CONTROL LOGIC		
ASSY NO. 181-6516-10 PCB PN 85-3222-01		
ENGINEER: R.M. NIEDZIELSKI	DATE: 08/18/86	
DRAWN BY: R.M.N.	SHEET 4 OF 12	REV: A
ZENITH	DATA SYSTEMS	St. Joseph, Michigan (616) 982-3200
(C) 1985 Zenith Data System		

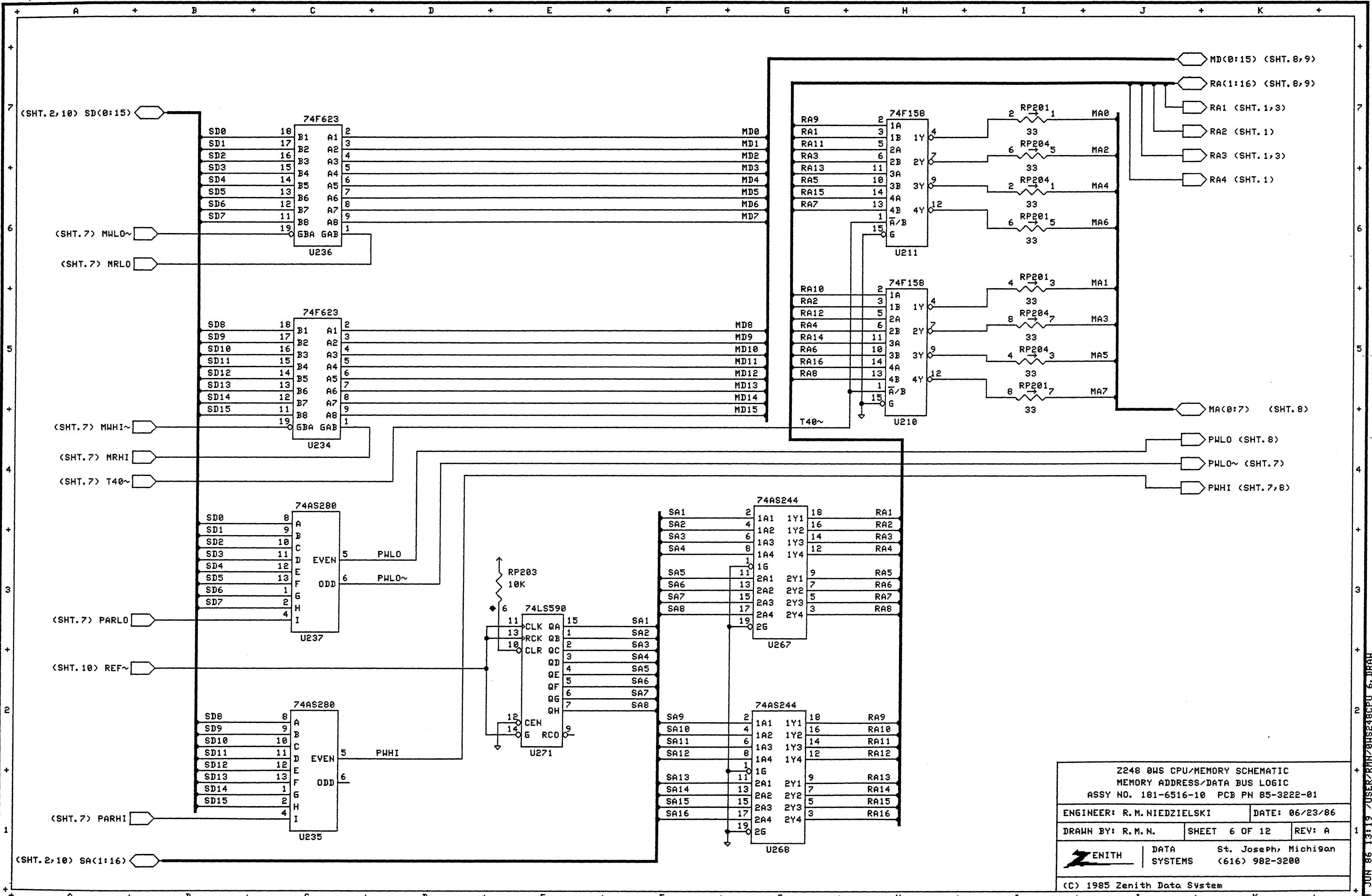
19 AUG 86 09:34 ZUSER/RMN/ONS248CPU 4. DRAN



Z248 0WS CPU/MEMORY SCHEMATIC  
 CPU DELAY & MISC. CONTROL LOGIC  
 ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 5 OF 12
DATA St. Joseph, Michigan SYSTEMS (616) 982-3200	
(C) 1985 Zenith Data System	

23 JUN 86 1318 7USER/RHN/GMS248CPU 5. DRAN



2248 SWS CPU/MEMORY SCHEMATIC  
 MEMORY ADDRESS/DATA BUS LOGIC  
 ASSY NO. 181-6516-10 PCB PN 85-3222-01

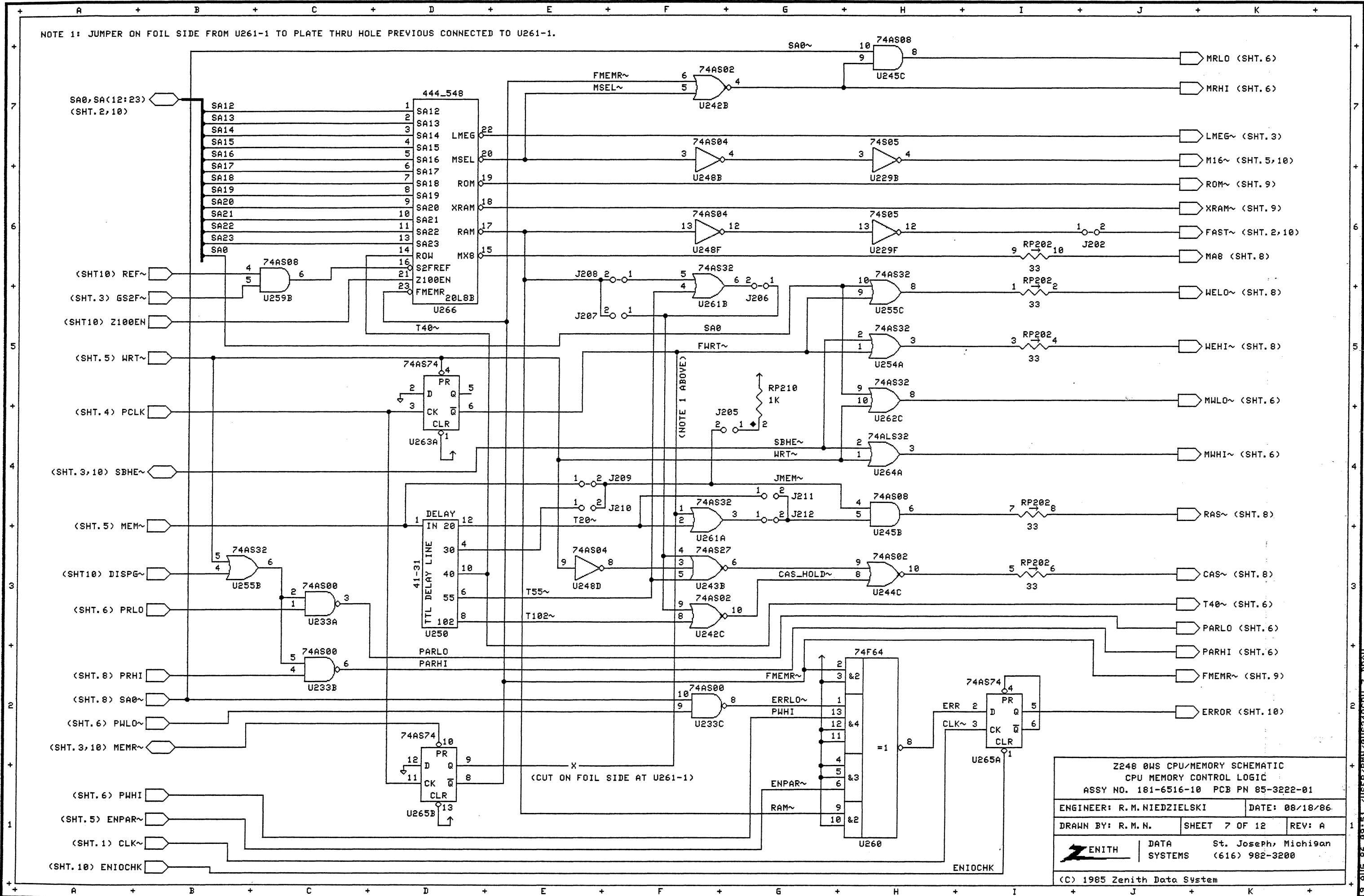
ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 6 OF 12 REV: A

**ZENITH** DATA St. Joseph, Michigan  
 SYSTEMS (616) 982-3200

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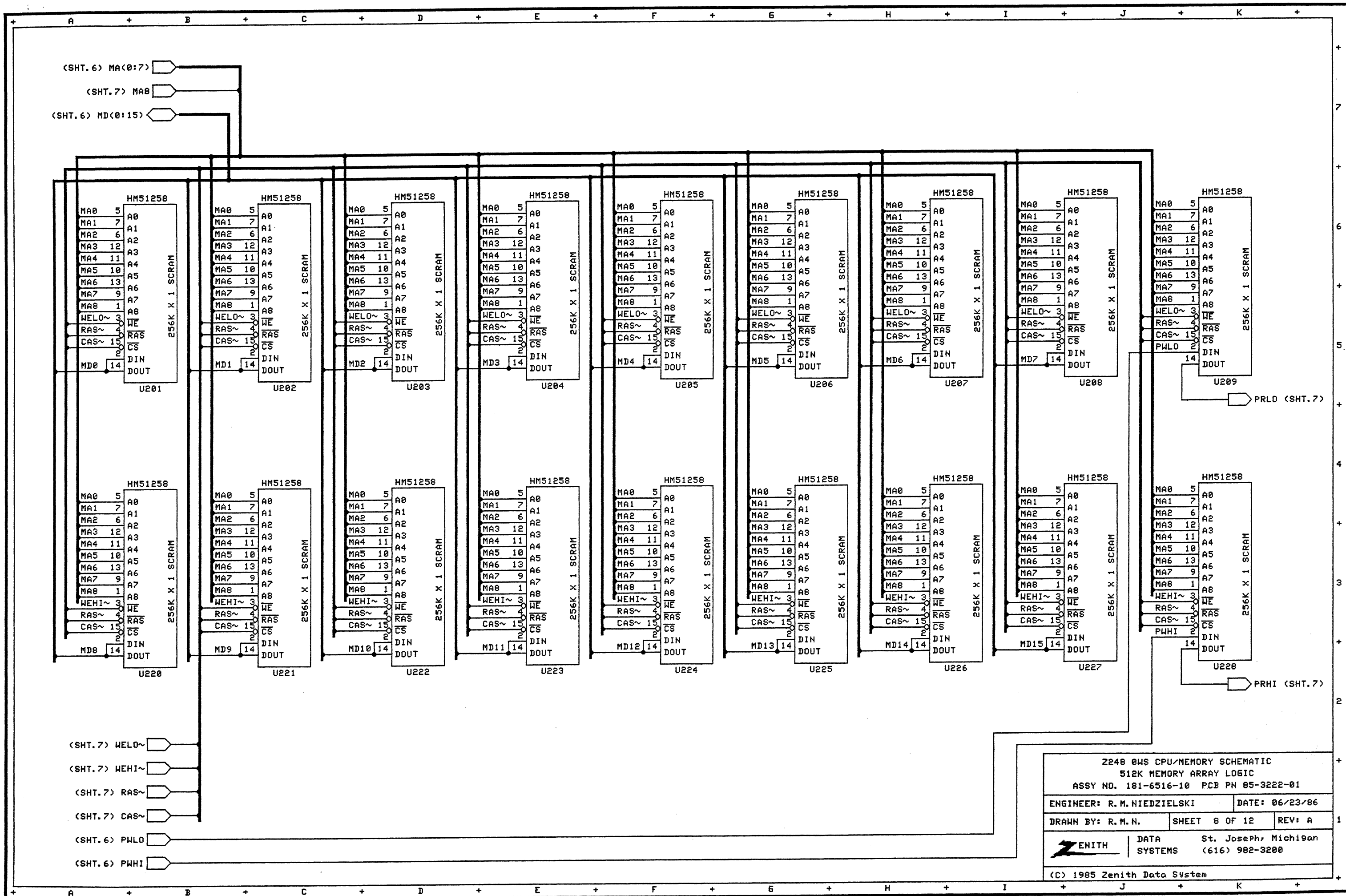
23 JUN 86 13:19 USER:RMN/085248CPU 6. DRAM

NOTE 1: JUMPER ON FOIL SIDE FROM U261-1 TO PLATE THRU HOLE PREVIOUS CONNECTED TO U261-1.



Z248 0WS CPU/MEMORY SCHEMATIC		
CPU MEMORY CONTROL LOGIC		
ASSY NO. 181-6516-10 PCB PN 85-3222-01		
ENGINEER: R. M. NIEDZIELSKI	DATE: 08/18/86	
DRAWN BY: R. M. N.	SHEET 7 OF 12	REV: A
<b>ZENITH</b> DATA SYSTEMS	St. Joseph, Michigan (616) 982-3200	
(C) 1985 Zenith Data System		

19 AUG 86 09:51 USER/RWN/0MS248CPU 7.DRAW



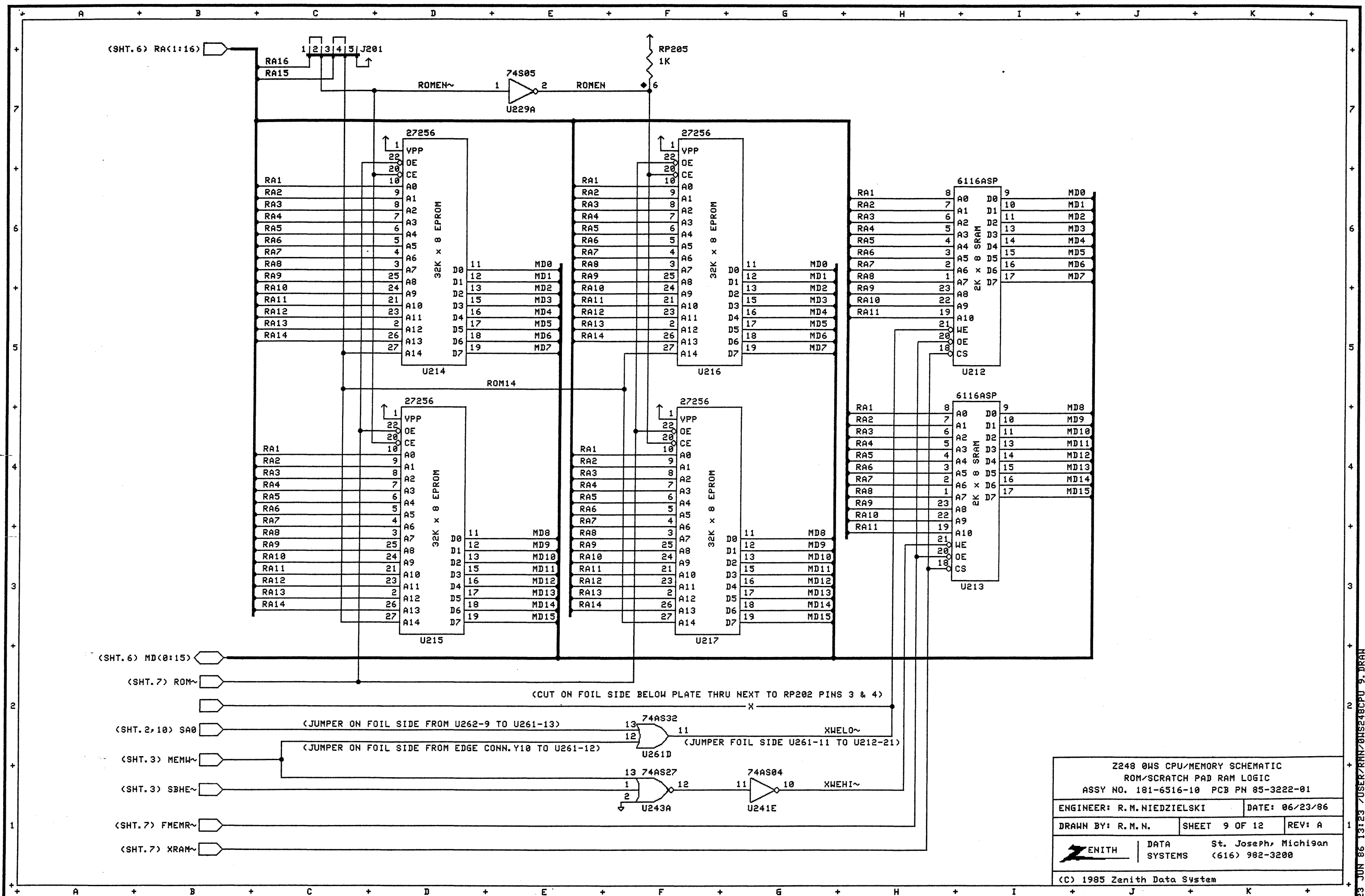
2248 0WS CPU/MEMORY SCHEMATIC  
512K MEMORY ARRAY LOGIC  
ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 8 OF 12
DATA St. Joseph, Michigan SYSTEMS (616) 982-3200	

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23 JUN 86 13:22 / USER/RMN/0NS248CPU 8. DRAM





Z248 QWS CPU/MEMORY SCHEMATIC  
 ROM/SCRATCH PAD RAM LOGIC  
 ASSY NO. 181-6516-10 PCB PH 85-3222-01

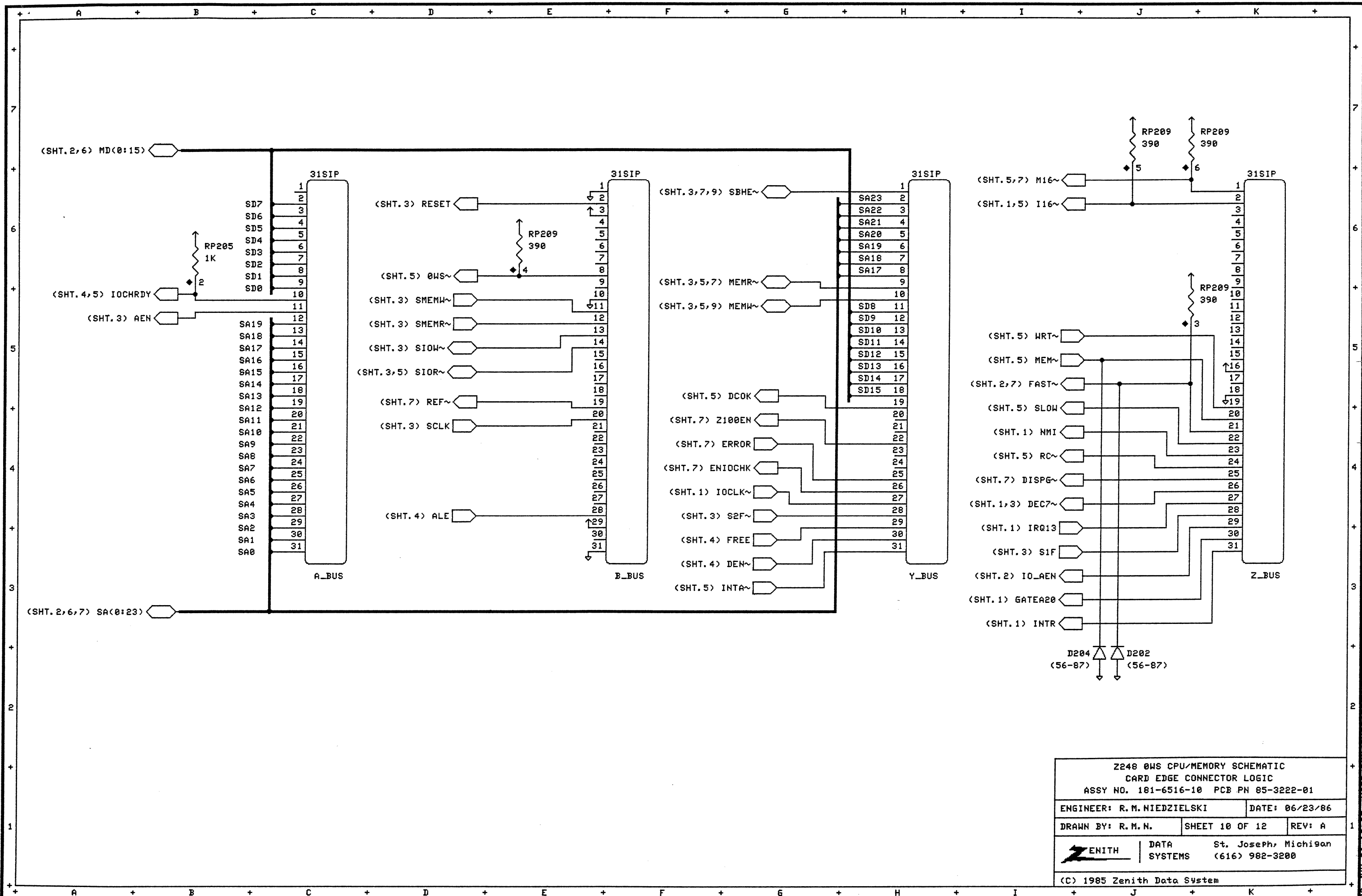
ENGINEER: R.M. NIEDZIELSKI      DATE: 06/23/86

DRAWN BY: R.M.N.      SHEET 9 OF 12      REV: A

ZENITH DATA SYSTEMS      St. Joseph, Michigan  
 (616) 982-3200

(C) 1985 Zenith Data System

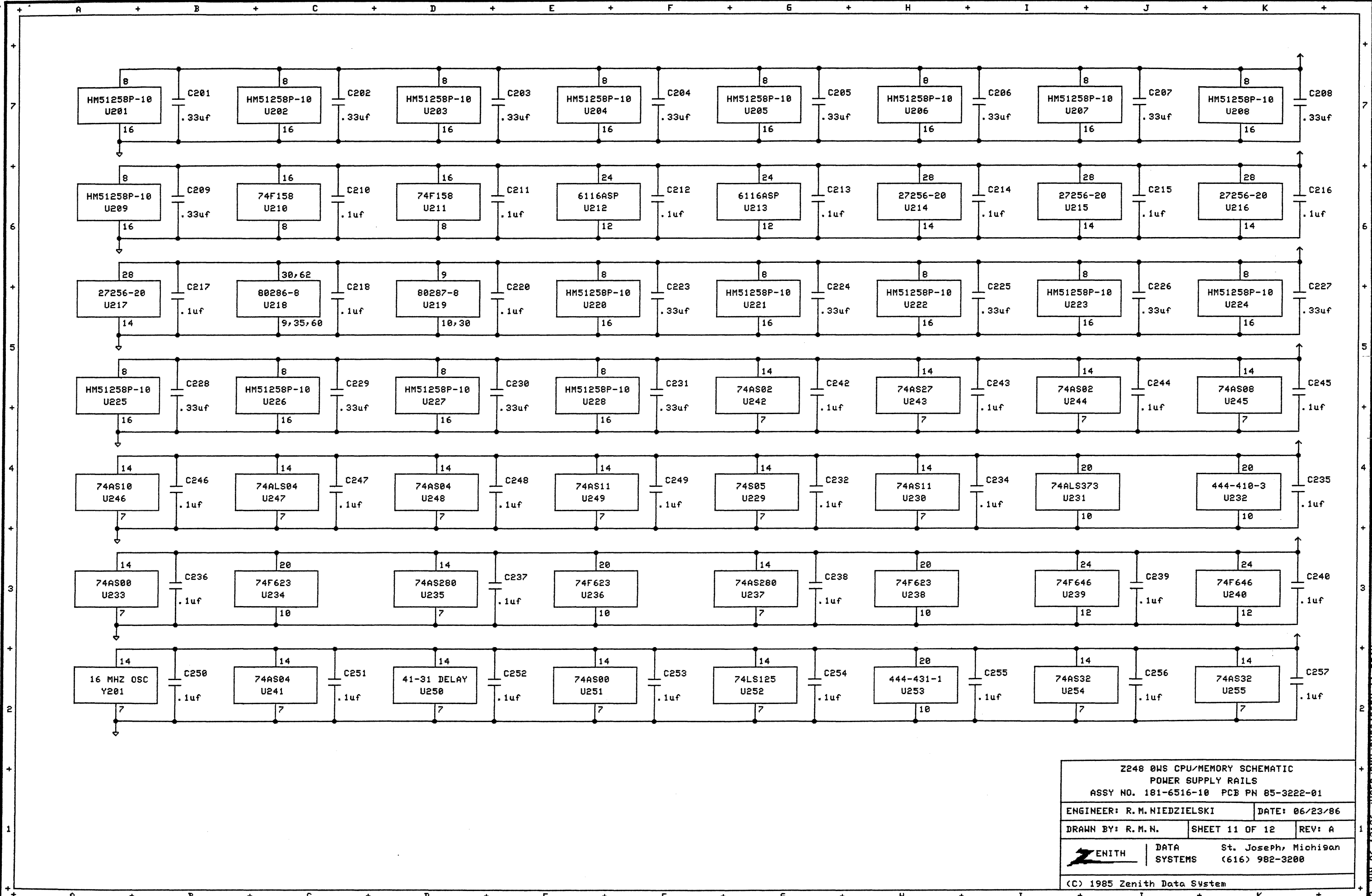
23 JUN 86 13:23 / USER:RMN/ONS248CPU 9. DRAM



**Z248 OWS CPU/MEMORY SCHEMATIC**  
**CARD EDGE CONNECTOR LOGIC**  
 ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 10 OF 12
<b>ZENITH DATA SYSTEMS</b> St. Joseph, Michigan (616) 982-3200	
(C) 1985 Zenith Data System	

23 JUN 86 13:25 USER/RMN/ONSE248CPU 10.DRAW



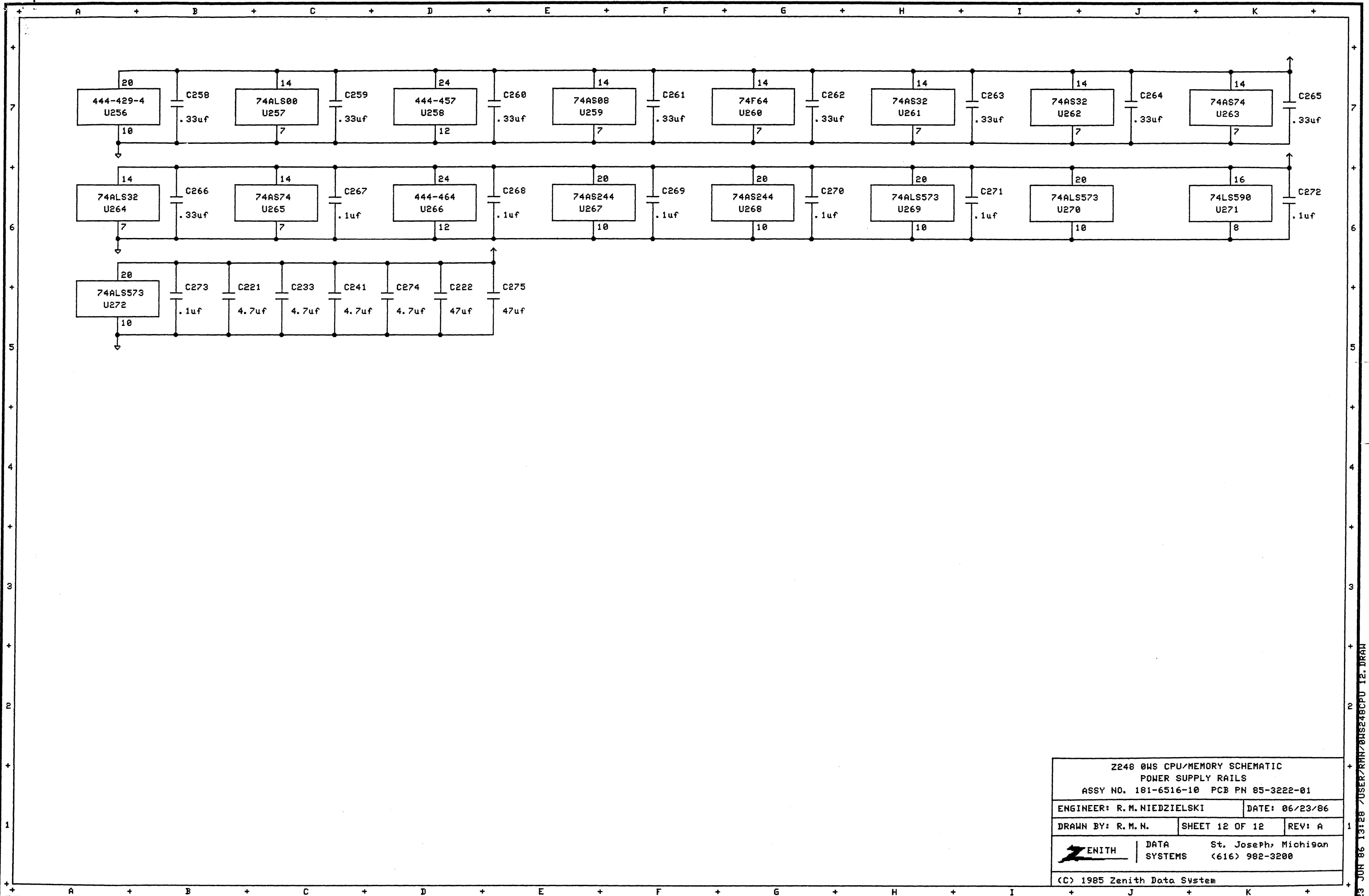
**Z248 0WS CPU/MEMORY SCHEMATIC**  
**POWER SUPPLY RAILS**  
 ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 11 OF 12 REV: A

**ZENITH DATA SYSTEMS**  
 St. Joseph, Michigan  
 (616) 982-3200

(C) 1985 Zenith Data System

23 JUN 86 13:26 70SER7RNN/0NS24BCPU 11.DRAW



Z248 OWS CPU/MEMORY SCHEMATIC  
 POWER SUPPLY RAILS  
 ASSY NO. 181-6516-10 PCB PN 85-3222-01

ENGINEER: R. M. NIEDZIELSKI	DATE: 06/23/86
DRAWN BY: R. M. N.	SHEET 12 OF 12 REV: A

**ZENITH** DATA St. Joseph, Michigan  
 SYSTEMS (616) 982-3200

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23 JUN 86 13:28 ZUSER7RNN70NS248CPU 12. DRAM